

FIG. 1 (PRIOR ART)

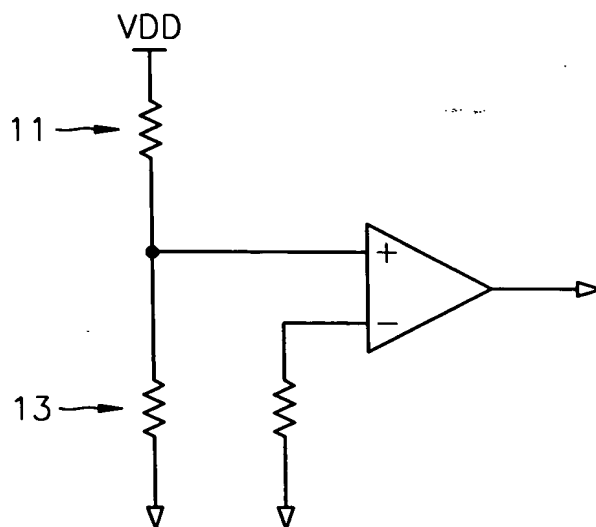


FIG. 2 (PRIOR ART)

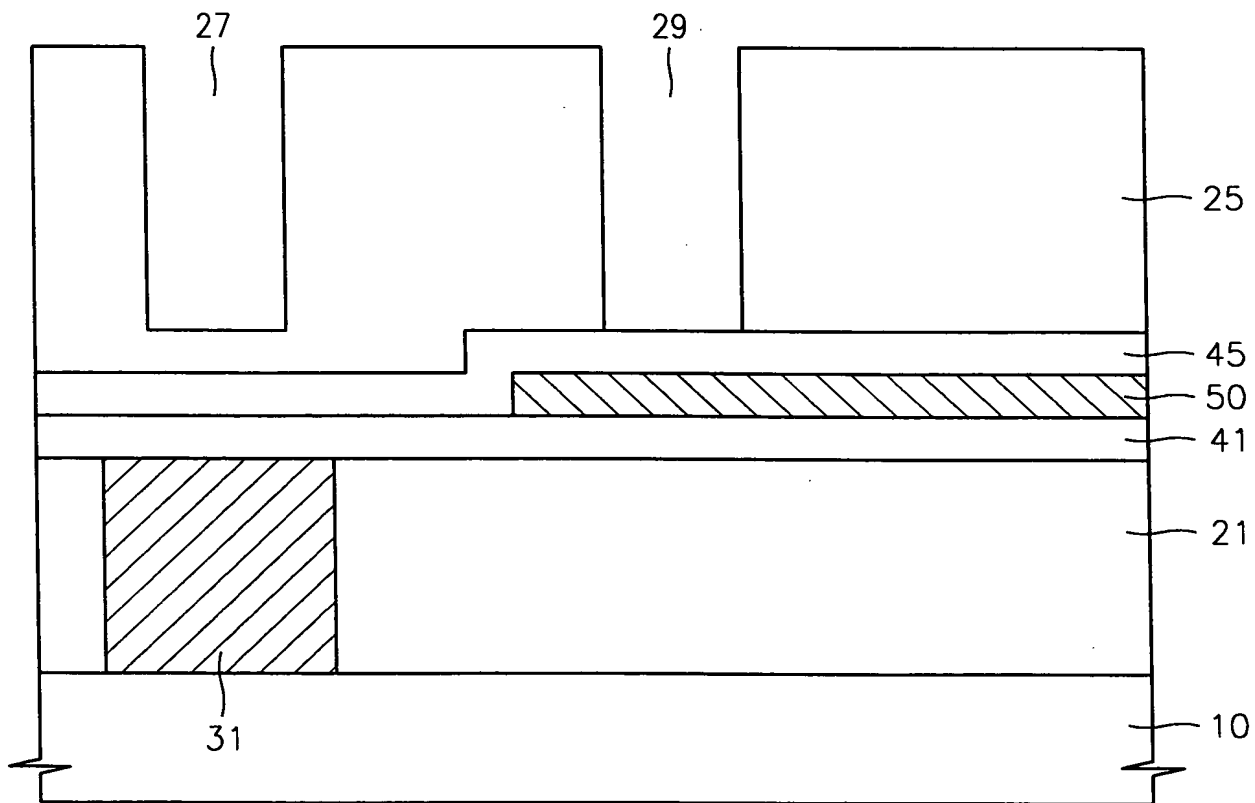


FIG. 3 (PRIOR ART)

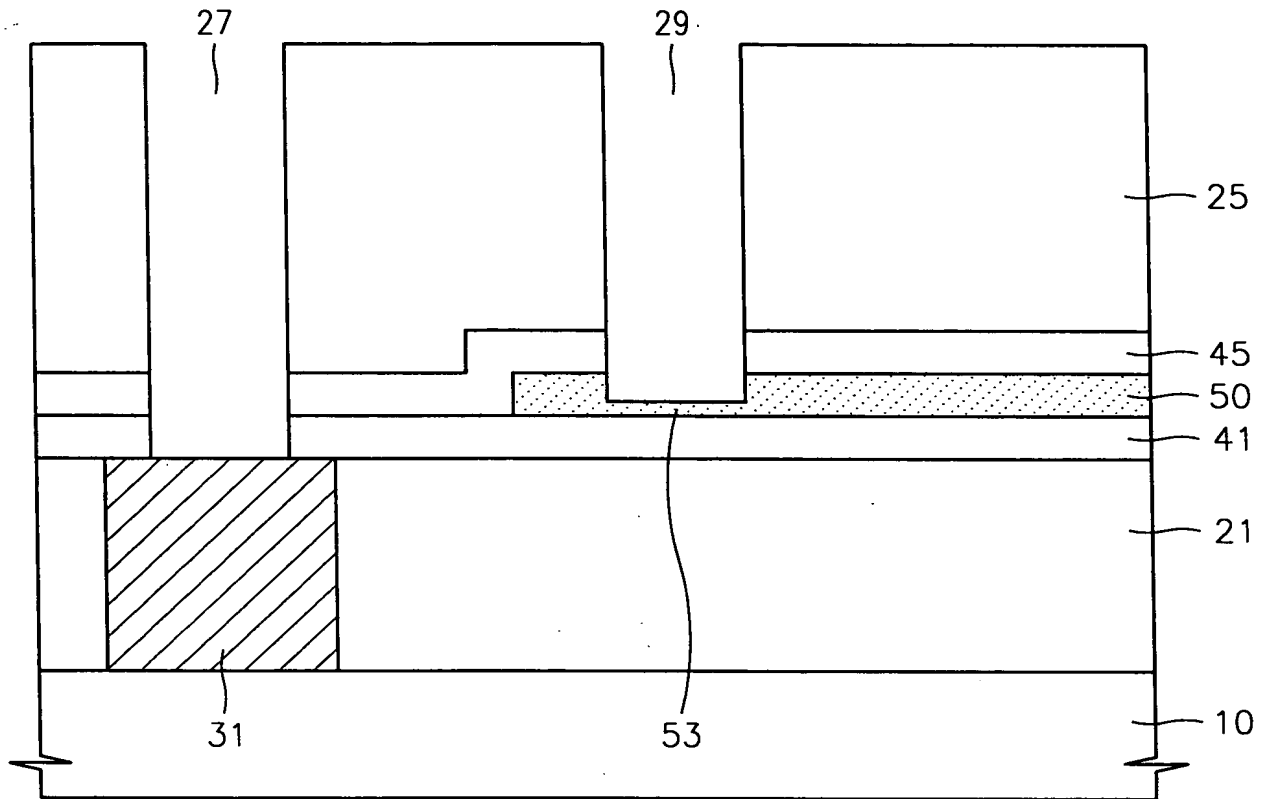


FIG. 4 (PRIOR ART)

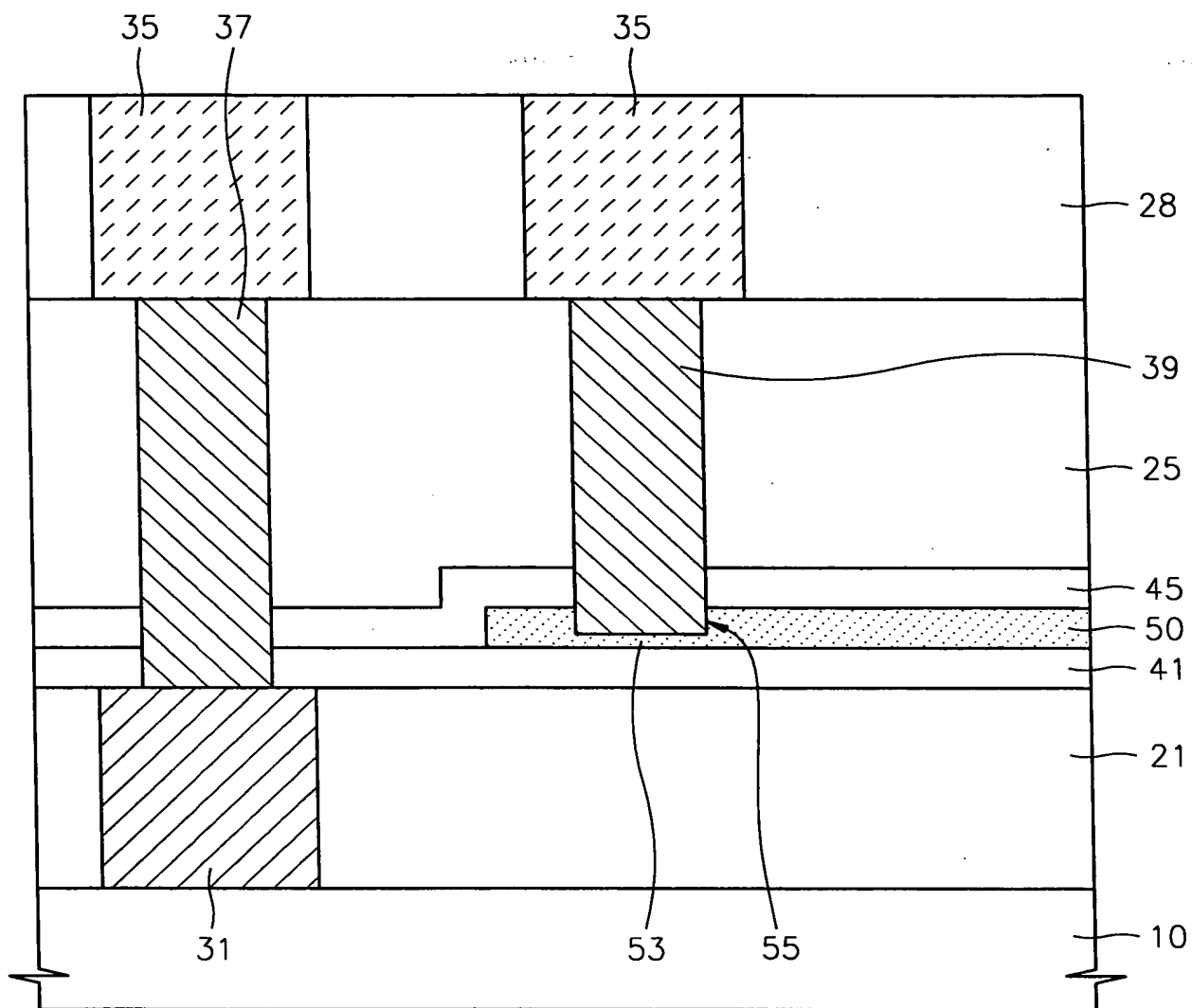


FIG. 5

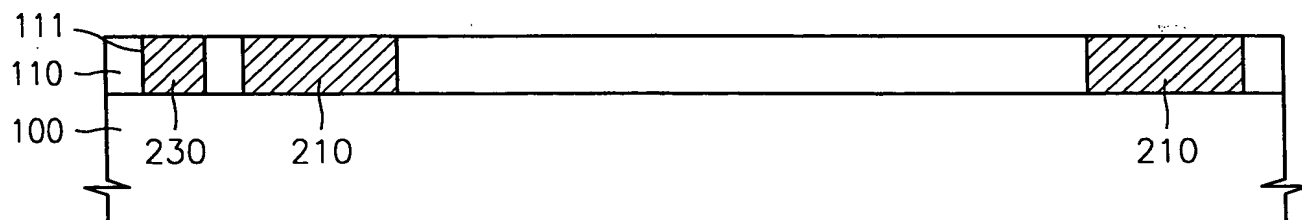


FIG. 6

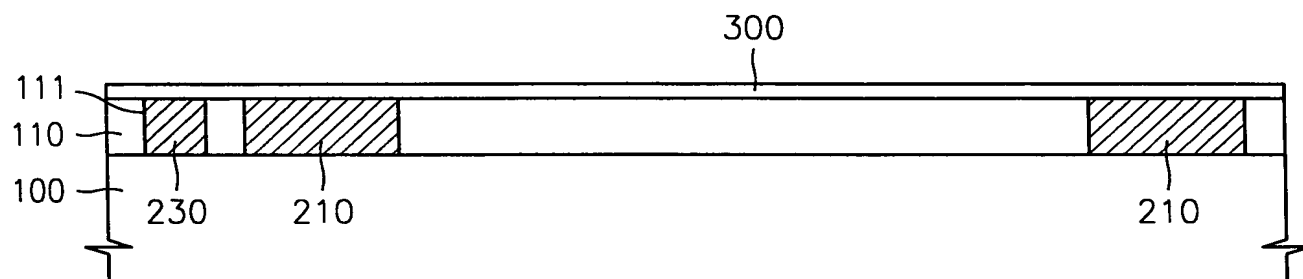


FIG. 7

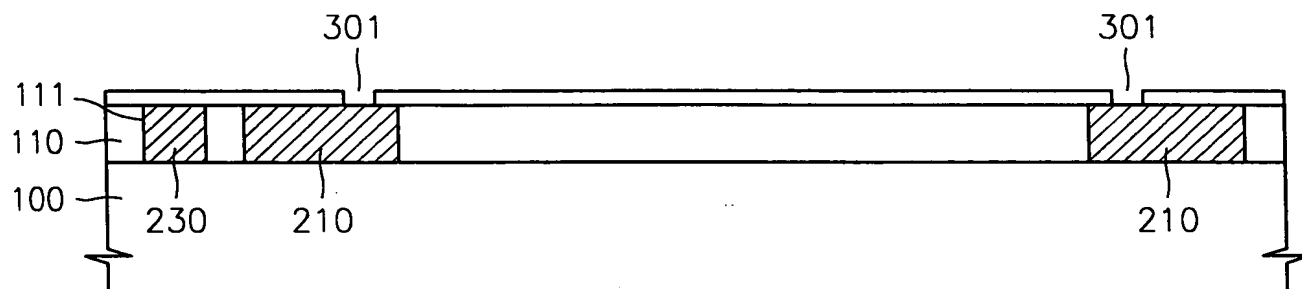


FIG. 8

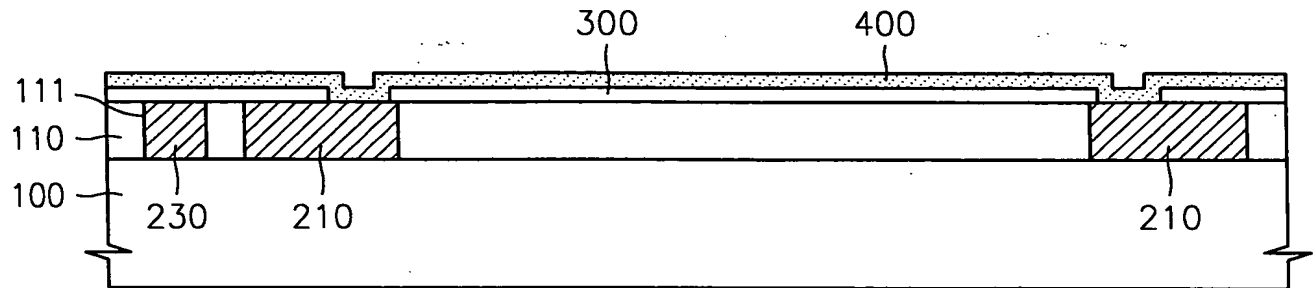


FIG. 9

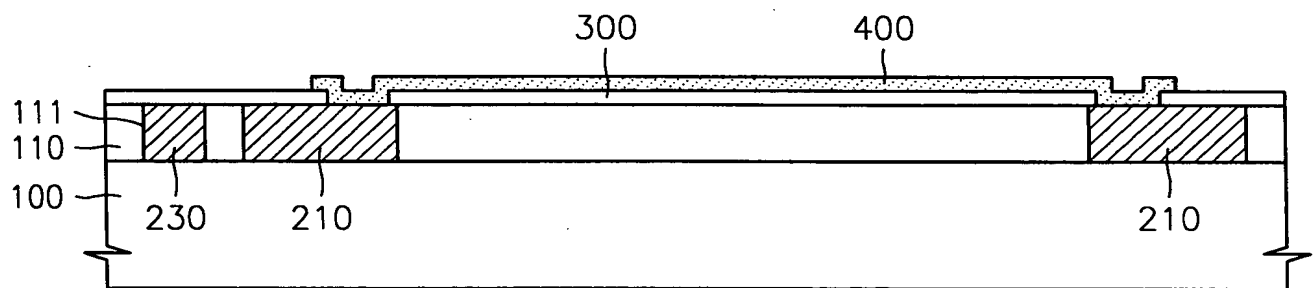


FIG. 10

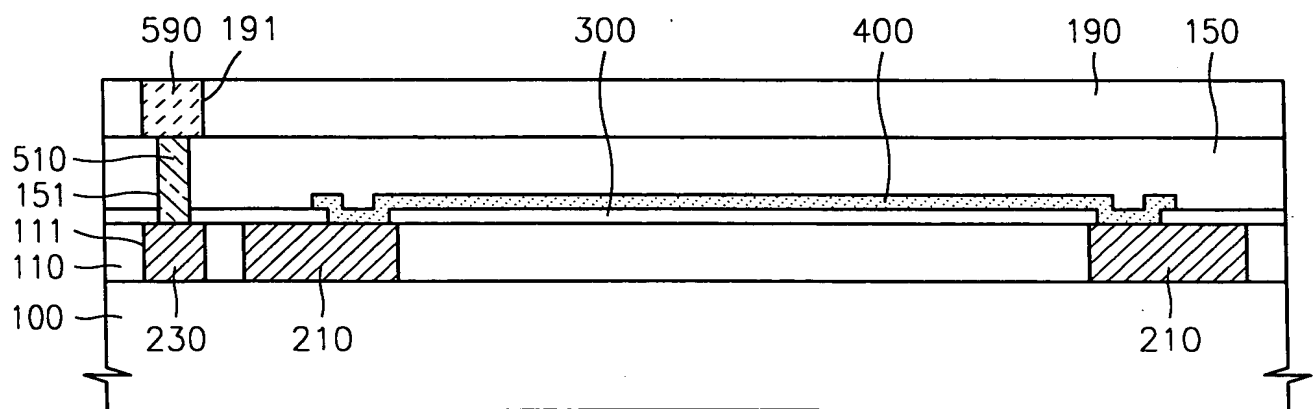


FIG. 11A

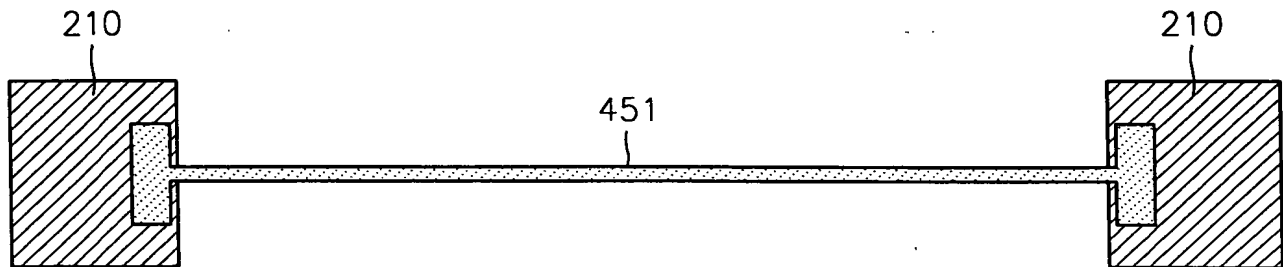
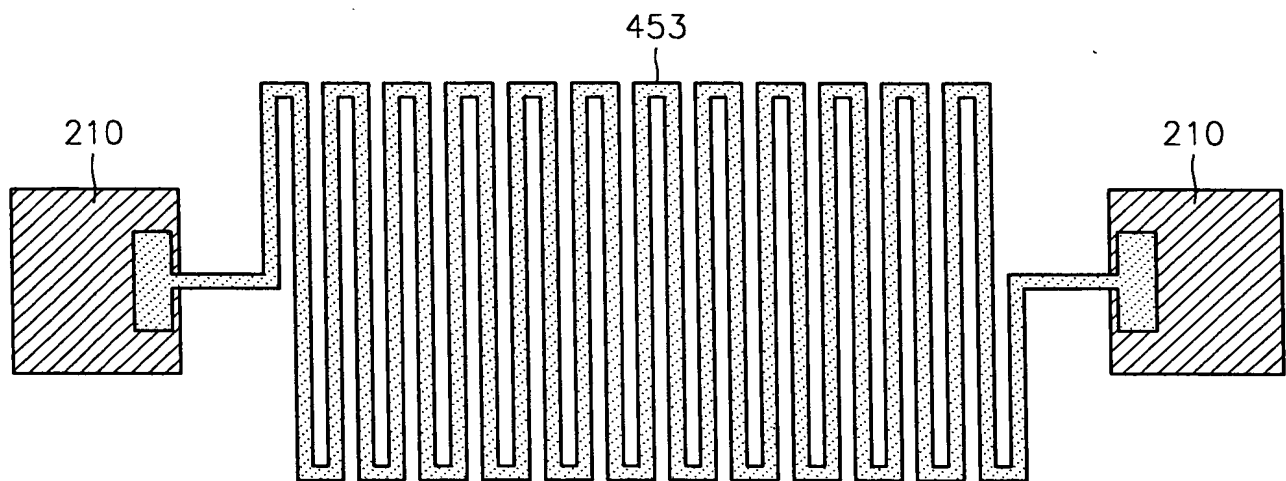


FIG. 11B



[illegible]

This cross-sectional view shows a semiconductor device. A gate stack is formed on a substrate, consisting of a gate dielectric layer (100) and a gate conductive layer (110). The gate conductive layer is patterned into a gate (115). A source/drain region (250) is formed in the substrate, adjacent to the gate. The source/drain region is covered by a source/drain dielectric layer (300). A source/drain contact (411) is formed in the source/drain dielectric layer, and a source/drain pad (400) is formed on top of the source/drain contact. The source/drain region is also covered by a source/drain conductive layer (210). The source/drain conductive layer is patterned into a source/drain contact (230) and a source/drain pad (210). The source/drain conductive layer is also covered by a source/drain dielectric layer (301).

FIG. 14

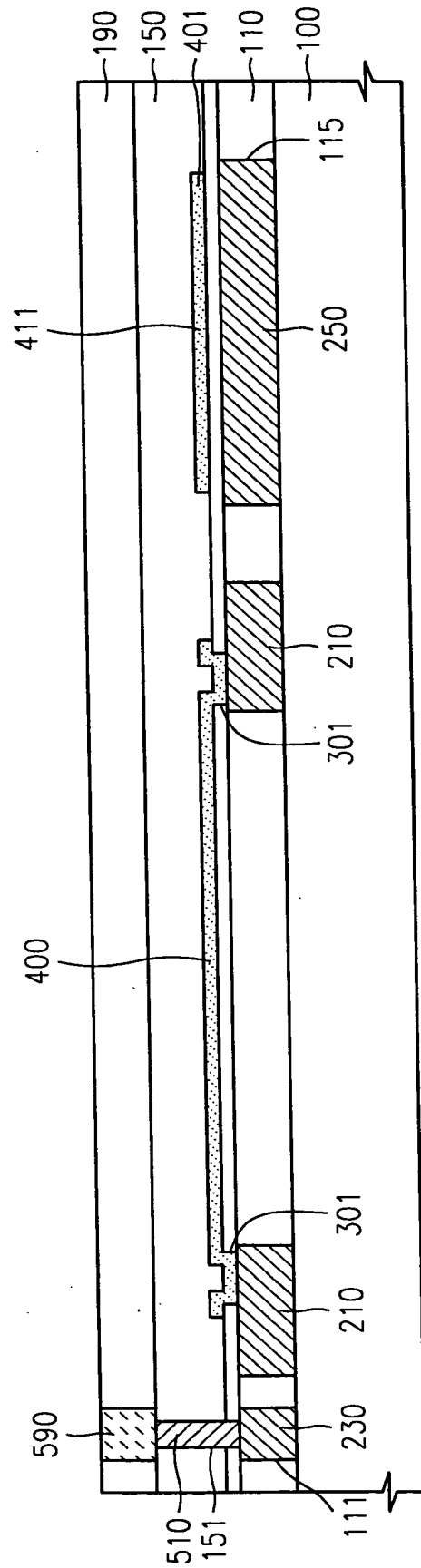
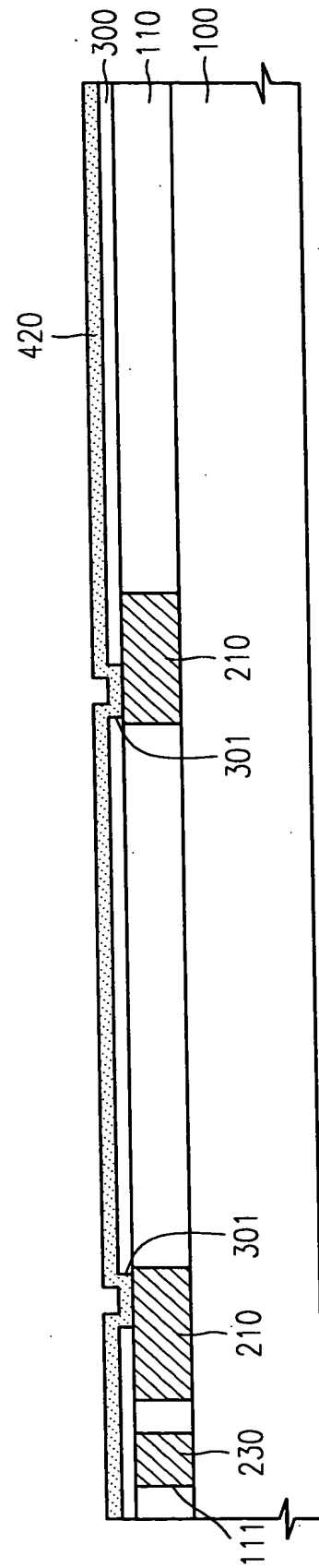


FIG. 15





[illegible]

This cross-sectional view shows a semiconductor device with a trench structure. The device includes a substrate 100 with a trench 110. A gate stack 111 is formed on the top surface of the substrate. The trench 110 is filled with a material 210. A layer 230 is formed on the bottom surface of the trench 110. A layer 301 is formed on the side walls of the trench 110. A layer 400 is formed on the top surface of the substrate. A layer 423 is formed on the top surface of the substrate. A layer 421 is formed on the top surface of the substrate. A layer 425 is formed on the top surface of the substrate. A layer 300 is formed on the top surface of the substrate. A layer 110 is formed on the top surface of the substrate. A layer 100 is formed on the top surface of the substrate.

This cross-sectional diagram illustrates a semiconductor device with a substrate 100. A series of layers are deposited on the substrate, including a layer 110, a layer 150, and a layer 190. A central region 400 is defined by a series of vertical lines, with sub-regions 421, 423, and 425. A layer 111 is located at the bottom of the device. A layer 210 is positioned above the central region 400. A layer 230 is located at the bottom of the device, adjacent to the substrate 100. A layer 301 is positioned above the layer 210. A layer 510 is located at the bottom of the device, adjacent to the substrate 100. A layer 590 is located at the bottom of the device, adjacent to the substrate 100.

FIG. 20

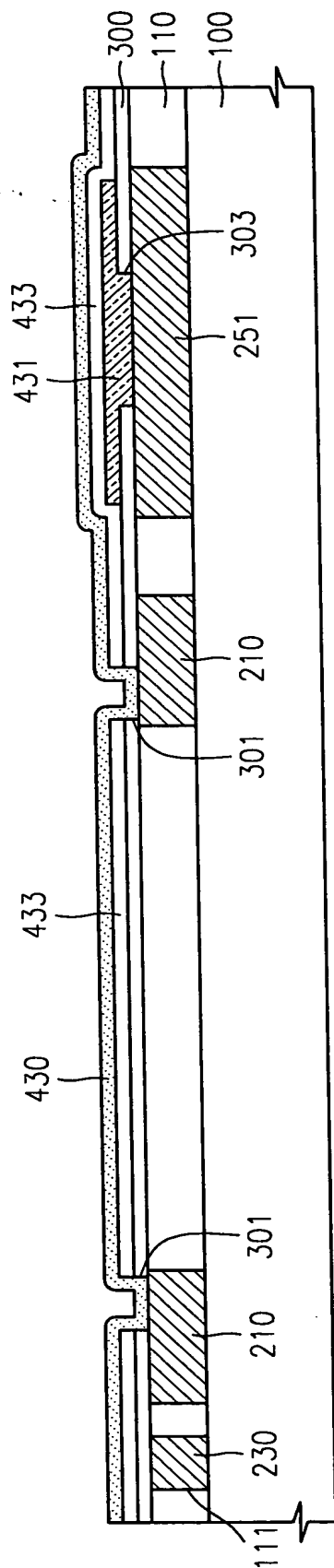
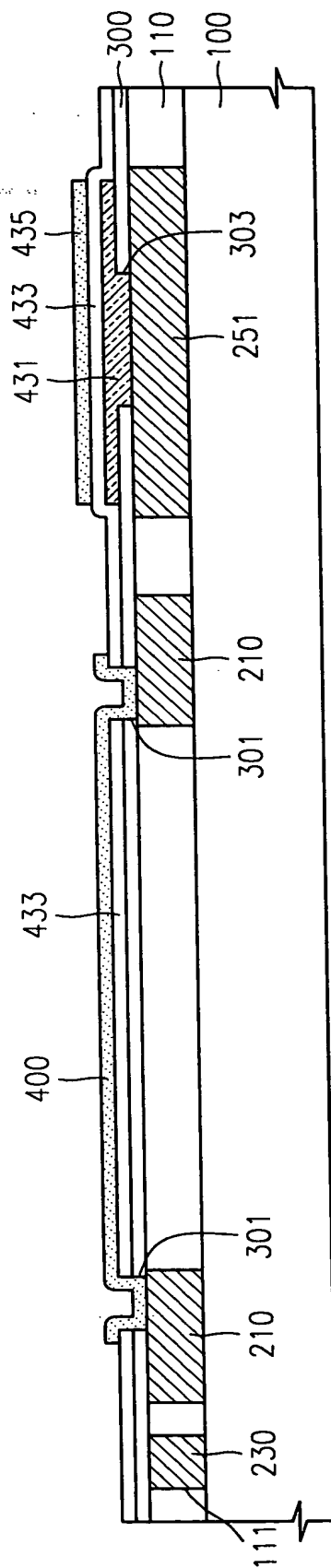


FIG. 21



This cross-sectional view shows a semiconductor device with a substrate 100. A first region 110 is defined by a first layer 111 and a second layer 115. A first contact 120 is formed in the first region 110. A first gate 130 is formed over the first contact 120. A first channel 140 is formed in the first region 110. A first source 150 is formed in the first region 110. A first drain 160 is formed in the first region 110. A first gate 170 is formed over the first drain 160. A first contact 180 is formed in the first region 110. A first layer 190 is formed over the first contact 180. A first region 200 is defined by a first layer 201 and a second layer 205. A first contact 210 is formed in the first region 200. A first gate 220 is formed over the first contact 210. A first channel 230 is formed in the first region 200. A first source 240 is formed in the first region 200. A first drain 250 is formed in the first region 200. A first gate 260 is formed over the first drain 250. A first contact 270 is formed in the first region 200. A first layer 280 is formed over the first contact 270. A first region 290 is defined by a first layer 291 and a second layer 295. A first contact 300 is formed in the first region 290. A first gate 310 is formed over the first contact 300. A first channel 320 is formed in the first region 290. A first source 330 is formed in the first region 290. A first drain 340 is formed in the first region 290. A first gate 350 is formed over the first drain 340. A first contact 360 is formed in the first region 290. A first layer 370 is formed over the first contact 360. A first region 380 is defined by a first layer 381 and a second layer 385. A first contact 390 is formed in the first region 380. A first gate 400 is formed over the first contact 390. A first channel 410 is formed in the first region 380. A first source 420 is formed in the first region 380. A first drain 430 is formed in the first region 380. A first gate 440 is formed over the first drain 430. A first contact 450 is formed in the first region 380. A first layer 460 is formed over the first contact 450. A first region 470 is defined by a first layer 471 and a second layer 475. A first contact 480 is formed in the first region 470. A first gate 490 is formed over the first contact 480. A first channel 500 is formed in the first region 470. A first source 510 is formed in the first region 470. A first drain 520 is formed in the first region 470. A first gate 530 is formed over the first drain 520. A first contact 540 is formed in the first region 470. A first layer 550 is formed over the first contact 540. A first region 560 is defined by a first layer 561 and a second layer 565. A first contact 570 is formed in the first region 560. A first gate 580 is formed over the first contact 570. A first channel 590 is formed in the first region 560. A first source 600 is formed in the first region 560. A first drain 610 is formed in the first region 560. A first gate 620 is formed over the first drain 610. A first contact 630 is formed in the first region 560. A first layer 640 is formed over the first contact 630. A first region 650 is defined by a first layer 651 and a second layer 655. A first contact 660 is formed in the first region 650. A first gate 670 is formed over the first contact 660. A first channel 680 is formed in the first region 650. A first source 690 is formed in the first region 650. A first drain 700 is formed in the first region 650. A first gate 710 is formed over the first drain 700. A first contact 720 is formed in the first region 650. A first layer 730 is formed over the first contact 720. A first region 740 is defined by a first layer 741 and a second layer 745. A first contact 750 is formed in the first region 740. A first gate 760 is formed over the first contact 750. A first channel 770 is formed in the first region 740. A first source 780 is formed in the first region 740. A first drain 790 is formed in the first region 740. A first gate 800 is formed over the first drain 790. A first contact 810 is formed in the first region 740. A first layer 820 is formed over the first contact 810. A first region 830 is defined by a first layer 831 and a second layer 835. A first contact 840 is formed in the first region 830. A first gate 850 is formed over the first contact 840. A first channel 860 is formed in the first region 830. A first source 870 is formed in the first region 830. A first drain 880 is formed in the first region 830. A first gate 890 is formed over the first drain 880. A first contact 900 is formed in the first region 830. A first layer 910 is formed over the first contact 900. A first region 920 is defined by a first layer 921 and a second layer 925. A first contact 930 is formed in the first region 920. A first gate 940 is formed over the first contact 930. A first channel 950 is formed in the first region 920. A first source 960 is formed in the first region 920. A first drain 970 is formed in the first region 920. A first gate 980 is formed over the first drain 970. A first contact 990 is formed in the first region 920. A first layer 1000 is formed over the first contact 990.

This cross-sectional view shows a multi-layered assembly. At the top, a thin layer 190 is on top of layer 150. Below these is a thick, hatched layer 300. A thin layer 110 is positioned between the hatched layer 300 and the bottom layer 100. The assembly is divided into three main sections by vertical interfaces. The left section contains layers 431, 433, and 435. The middle section contains layers 251, 303, 270, 305, 210, and 301. The right section contains layers 435', 431', 210, 301, 270, 305, and 301. A hatched layer 590 is located at the bottom left, adjacent to layer 510. A small layer 151 is also visible at the bottom left.

FIG. 24

